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## ULTRA LINEAR HIGH SPEED OPERATIONAL AMPLIFIER OUTPUT STAGE

### Technical Field of the Invention

10 This invention generally relates to electronic systems and in particular to  
operational amplifier output stages.

### Background of the Invention

Operational amplifiers are used in many electronic circuits to condition,  
manipulate and amplify signals. The operating characteristics of a particular  
15 operational amplifier are dependent upon its circuit topology. Generally, the  
operational amplifier consists of a number of stages, each containing internal sub-  
stages.

5 Crossover distortion is an important parameter op-amp performance and is largely correlated to bias current. It occurs, for example, when a signal being processed in a class AB amplifier transitions from the positive portion of a cycle to the negative portion of a cycle, and the reverse. This distortion is primarily generated in output transistors. To minimize crossover distortion, transistors within  
10 operational amplifier output stage circuits are sometimes biased slightly above cut-off. The class AB biasing arrangement consumes more power than if the transistors are biased in a class B configuration, but result in less cross-over distortion. The class AB biasing arrangement has more cross-over distortion than a class A biasing arrangement, but uses less current for proper operation.

15 Summary of the Invention

The present invention achieves technical advantages as an ultra linear high speed operational amplifier output stage using a localized feedback system in which current gains are close to  $\beta_n \cdot \beta_p$ , where  $\beta_n$  refers to the beta of either the pre-driver npn transistor, output driver npn transistor or an average of both, depending on the  
20 current signal and  $\beta_p$  refers to the beta of either the pre-driver pnp transistor, output pnp transistor or an average of both. Where signal current is large and positive, load conduction is through the output npn transistor and pre-driver pnp transistor. Where signal current is large and negative, load conduction is through the pre-driver npn transistor and output pnp transistor. Where the signal is small, load conduction

5 varies in tandem through the output npn transistor and pre-driver pnp transistor and the output pnp transistor and pre-driver npn transistor.

The output stage can be seen to comprise a pre-driver sub-stage and final sub-stage. The pre-driver sub-stage is further comprised of a first and a second pre-driver sub-stage circuit. In addition, the final sub-stage is further comprised of a first and a second final sub-stage circuit. The input to the present invention comprises a transconductance (" $g_m$ ") cell which, when a voltage is applied thereto, an error voltage appears across the input  $g_m$  cell and an error current is produced at the output of the input  $g_m$  cell. The error current ( $\delta I_{in}$ ) flows into the emitters of two pre-driver sub-stage transistors and flows out of their collectors into the bases of two other pre-driver transistors. Through this translinear loop, no net signal is lost. The gained up error currents then flow into the final sub-stage translinear loop, specifically, into the bases of two final sub-stage transistors. Effectively, in the small signal context, the first pre-driver sub-stage circuit amplifies a positive portion of the current signal for output to the first final sub-stage circuit while the second pre-driver sub-stage circuit amplifies a negative portion of the current signal for output to the second final sub-stage circuit. The first and second final sub-stages further amplify the positive portion and negative portion, respectively, of the current signal.

5           The first and second final sub-stage circuits are interconnected at an output terminal of the operational amplifier output stage such that the amplified positive portion of the signal and amplified negative portion of the signal are joined substantially in phase with improved crossover distortion characteristics.

Brief Description of the Drawings

10           For a more complete understanding of the present invention, reference is made to the detailed description taken in conjunction with the following drawings:

Figure 1 is a circuit diagram of a first conventional operational amplifier output stage;

Figure 2 is a circuit diagram of a second conventional operational amplifier  
15   output stage;

Figure 3 is a graph illustrating the linearity characteristics of the first conventional operational amplifier. This figure shows the first derivative ( $\delta V_o / \delta V_i$ ) of the amplifier's DC transfer characteristic;

5           Figure 4 is a graph illustrating the linearity characteristics of the second conventional operational amplifier. This figure shows the first derivative ( $\delta V_o/\delta V_i$ ) of the amplifier's DC transfer characteristic;

          Figure 5 shows the single ended and differential linearity characteristics of the first conventional operational amplifier output stage using a discrete multi-tone  
10 ("DMT") signal with missing tones;

          Figure 6 is a graph illustrating the typical linearity characteristics of the first conventional operational amplifier output stage in harmonic distortion form;

          Figure 7 is a circuit diagram of a first embodiment of the present invention with a  $g_m$  cell input;

15           Figure 8 is a circuit diagram of a second embodiment of the present invention with a  $g_m$  cell input;

          Figure 9 is a graph illustrating the linearity characteristics of the first embodiment of the present invention. This figure shows the first derivative ( $\delta V_o/\delta V_i$ ) of the amplifier's DC transfer characteristic;

5           Figure 10 is a graph illustrating the linearity characteristics of the first embodiment of the present invention using a DMT signal with missing tones;

          Figure 11 is a graph illustrating the linearity characteristics of the first embodiment of the present invention in harmonic distortion form;

          Figure 12 illustrates the translinear loop formed by the first, second, third and  
10   fourth transistors;

          Figure 13 illustrates the translinear loop formed by the fifth, sixth, seventh and eight transistors;

          Figure 14 is a circuit diagram of the final sub-stage of the first embodiment of the present invention using type I biasing of the output transistors in a no-load  
15   configuration;

          Figure 15 is a circuit diagram of the final sub-stage of the first embodiment of the present invention using type I biasing of the output transistors with a load;

          Figure 16 is a graph illustrating the current gain of the final sub-stage of the first embodiment of the present invention;

5           Figure 17 is a circuit diagram of the final sub-stage of the second embodiment of the present invention using type II biasing of the output transistors in a no load configuration;

          Figure 18 is a circuit diagram of the final sub-stage of the second embodiment of the present invention using type II biasing of the output transistors  
10   with a signal applied to such final sub-stage's input;

          Figure 19 is a graph illustrating the DC current transfer characteristic of the final sub-stage of Figure 18;

          Figure 20 is a graph illustrating the DC current transfer characteristic of the final sub-stage of Figure 15;

15           Figure 21 is a graph illustrating the linearity characteristic of the final sub-stage of Figure 15 and Figure 18. This figure shows the first derivative ( $\delta I_o / \delta I_i$ ) of the amplifiers' DC current transfer characteristics;

          Figure 22 is a circuit diagram of a conventional operational amplifier illustrating bias setup for the output transistors;

5           Figure 23 is a graph illustrating the DC current transfer characteristics of  
circuit depicted in Figure 22;

          Figure 24 is a circuit diagram of the first embodiment of the present invention  
with current feedback circuitry;

          Figure 25 is a circuit diagram of the first embodiment of the present invention  
10   with voltage feedback circuitry;

          Figure 26 is a circuit diagram of the second embodiment of the present  
invention with current feedback;

          Figure 27 is a circuit diagram of the second embodiment of the present  
invention with voltage feedback;

15           Figure 28 is a graph comparing the linearity characteristics between the two  
conventional operational amplifiers and the first and second embodiments of the  
present invention. The figure shows the first derivative of the amplifiers' gain.

          Figure 29 is a circuit diagram of the first embodiment of the present invention  
with a compound darlington output stage using type I biasing;

5           Figure 30 is a circuit diagram of the first embodiment of the present invention with a compound darlington output stage using type I biasing and a differential pair input  $g_m$  cell;

Figure 31 is a circuit diagram illustrating a current feedback stability loop;

Figure 32 is a circuit diagram implementing conventional Miller  
10   compensation using a current feedback with the embodiments of the present invention;

Figure 33 is a circuit diagram illustrating a voltage feedback stability loop;

Figure 34 is a circuit diagram illustrating implementation of conventional  
Miller compensation using voltage feedback to achieve right-half-plane zero  
15   ("RHPZ") cancellation with the embodiments of the present invention; and

Figure 35 is a circuit diagram illustrating a method for achieving low frequency precision in either of the first or second embodiments of the present invention.

5           Description of Conventional Amplifier Output Stages

Figure 1 is a circuit diagram of a first conventional operational amplifier output stage. Figure 2 is a circuit diagram of a second conventional operational amplifier output stage. Figure 3 illustrates the linearity characteristics of such first conventional operational amplifier by showing the first derivative of the DC transfer characteristic. Figure 4 illustrates the linearity of such second conventional operational amplifier by showing the first derivative of the DC transfer characteristic. Figure 5 illustrates the single ended and differential linearity of such first conventional operational amplifier with a discrete multi tone ("DMT") signal with missing tones. DMT signal is a broadband signal containing many sinusoids spaced at equal intervals. The missing tone performance looks for intermodulation products from the broadband DMT signal in at a frequency where there is no sinewave present in the DMT signal. DMT is a rigorous test of an amplifier's linearity. Figure 6 illustrates the typical linearity of such first and second conventional operational amplifiers in harmonic distortion form.

10  
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20           Detailed Description of the Present Invention

Two embodiments of the present invention are shown in Figures 7 and 8. As compared to the conventional operational amplifier output stages as disclosed in Figures 1 and 2, the disclosed embodiments of an operational amplifier output stage as shown in Figures 7 and 8, has higher linearity using the equivalent biasing current,

5 or alternatively, the same linearity with lower biasing current. The operational amplifier output stage disclosed herein significantly reduces crossover distortion and reduces current use during operation. Further, because frequency response of a conventional amplifier output stage is sometimes reduced to lower the amount of biasing current needed during operation, the disclosed invention also has the  
10 advantage of extended bandwidth. The disclosed operational amplifier output stage comprises a pre-driver sub-stage utilizing translinear current loops and a final sub-stage. The final sub-stage of the operational amplifier output stage disclosed herein comprises a complementary set of compound darlington transistors enclosed in a localized feedback system.

15 As used herein, translinearity refers to the characteristics of non-linear circuits whose operation is based on the exponential current-voltage relationship of the bipolar junction transistor;  $\beta$  refers to the ratio of DC collector current to DC base current in a bipolar junction transistor or current gain from base to collector;  $\alpha$  represents the fraction of signal current going into one half of the pre-driver sub-  
20 stage,  $\lambda$  refers to the fraction of signal current going into the other half of the pre-driver sub-stage, and A refers to the emitter area of the BJT in consideration.

Figure 7 is a circuit diagram of the first embodiment of an operational amplifier output stage having reduced supply current and high linearity constructed

5 according to the teachings of the present invention. The circuit 100 includes an input  
g<sub>m</sub> cell 121, pre-driver sub-stage comprised of eight pre-driver sub-stage transistors  
101, 102, 103, 104, 105, 106, 107 and 108, a final sub-stage comprising four final  
sub-stage transistors 109, 110, 111 and 112, and four current sources 131, 132, 133  
and 134. The input g<sub>m</sub> cell 121 is configured to accept an input voltage signal,  
10 produce an error voltage across its input, and produce an output error current ( $\delta I_{in}$ ).

As shown therein, a first voltage supply rail 41 is coupled to a first node 51, a  
second voltage supply rail 42 is coupled to a fifth node 55.

The first pre-driver sub-stage circuit consists of four transistors 101, 102, 103  
and 104. In the first pre-driver sub-stage circuit, the emitter of the first transistor 101  
15 is coupled to the first voltage supply rail 41 at the first node 51, and the base of the  
first transistor 101 is coupled to a second node 52. The emitter of the second  
transistor 102 is also coupled to the second node 52; and its base is coupled to a third  
node 53. The base and collector of the third transistor 103 are also coupled to the  
third node 53. The collector and base of the fourth transistor 104 are each coupled to  
20 a fourth node 54. The emitter of the fourth transistor 104 is coupled to the voltage  
supply rail 41 at the first node 51.

5           The second pre-driver sub-stage circuit comprises four transistors 105, 106,  
107 and 108. The second voltage supply rail 42 is coupled to the fifth node 55. The  
emitter of the fifth transistor 105 is coupled to the second voltage supply rail 42 at  
the fifth node 55 and its base is coupled to a the sixth node 56. The emitter of the  
sixth transistor 106 is coupled to the sixth node 56 and its base is coupled to a  
10 seventh node 57. The collector of the sixth transistor 106 is coupled to the second  
node 52. The base and collector of the seventh transistor 107 are coupled to a  
seventh node 57 and its emitter is coupled to an eighth node 58. The collector and  
base of the eighth transistor 108 are coupled to the eighth node 58, and the emitter of  
the eighth transistor 108 is coupled to the second voltage supply rail 42 at the fifth  
15 node 55.

          The collector of the second transistor 102 and the emitter of the sixth  
transistor 106 are coupled to a common sixth node 56. The emitter of the second  
transistor 102 and the emitter of the sixth transistor 106 are coupled to a common  
second node 52. The cross connection advantageously results in no error current  
20 being lost in the translinear loops.

          A first current source 131 is coupled to the first voltage supply rail 41 at the  
first node 51 and at the second node 52. A second current source 132 is coupled to  
the first voltage supply rail 41 at the first node 51 and at the seventh node 57. A third

5 current source 133 is coupled to the second voltage supply rail 42 at the fifth node 55 and at the third node 53. A fourth current source 134 is coupled to the voltage supply rail 42 at the fifth node 55 and at the sixth node 56.

The final sub-stage 123 comprises a complementary pair of darlington transistors. The first set of darlington transistors is comprised of the ninth and tenth  
10 transistors 109 and 110. The emitter of the ninth transistor 109 is coupled to the collector of the first transistor 101 at a ninth node 59. The base and collector of the ninth transistor 109 are coupled at a tenth node 60. The base of the tenth transistor 110 is coupled to the ninth node 59, and the collector of the tenth transistor 110 is coupled to the first voltage supply rail 41 at the first node 51.

15 The second set of darlington transistors is comprised of the eleventh and twelfth transistors 111 and 112. The emitter of the eleventh transistor 111 is coupled to the collector of the fifth transistor 105 at an eleventh node 61. The base and collector of the eleventh transistor 111 are coupled to the base and collector of the ninth transistor 109 at the tenth node 60. The base of the twelfth transistor 112 is  
20 coupled to the eleventh node 61, and the collector of the twelfth transistor 112 is coupled to the second voltage supply rail 42 at the fifth node 55. The twelfth node 62 couples the emitter of the tenth transistor 110 to the emitter of the twelfth transistor 112. An output terminal 91 is coupled to the twelfth node 62. The twelfth

5 node 62 also interconnects the output terminal 91 to the  $g_m$  cell input 121. The configuration of the ninth transistor 109 and eleventh transistor 111 of the first embodiment of the present invention is also referred to as type I biasing.

A second embodiment of the present invention is disclosed in Figure 8. The second embodiment is also referred to as type II biasing of the output transistors. In  
10 this second embodiment, the collectors of the ninth transistor 109 and the eleventh transistor 111 are not coupled at the tenth node 60. The collector of the ninth transistor 109 is coupled to the second voltage supply rail  $V_{cc}$  42 at the fifth node 55 and the collector of the eleventh transistor 111 is coupled to the first voltage supply rail  $V_{cc}$  41 at the first node 51. In this case the current gain from the collectors of  
15 101 or 105 to the output node 91 is the average of  $\beta_n$  and  $\beta_p$ . This arrangement minimizes crossover distortion in the output signal. As used herein,  $\beta_n$  refers to the beta of transistor 110 and  $\beta_p$  refers to the beta of transistor 101, where  $\alpha = 1$  and  $\lambda = 1$ ; or  $\beta_n$  refers to the beta of transistor 105 and  $\beta_p$  refers to the beta of transistor 112, where  $\alpha = 0$  and  $\lambda = 0$ , or, in the small signal context, where  $\alpha = .5$  and  $\lambda = .5$ ,  $\beta_n$   
20 refers to the average of the beta of transistor 110 and transistor 105 and  $\beta_p$  refers to the beta of the average of transistor 101 and transistor 112, the relative contribution of each such pnp transistor and npn transistor to  $B_n$  and  $B_p$  varying proportionally with the variation in  $\alpha$  and  $\lambda$ .

5           Figures 9, 10 and 11 illustrate different performance aspects of the present invention. Specifically, Figure 9 shows the linearity characteristics of the first embodiment of the present invention, specifically the first derivative ( $\delta V_o / \delta V_i$ ) of the amplifier's DC transfer characteristic. Figure 10 shows the linearity characteristics of the first embodiment of the present invention using a DMT signal with missing  
10 tones. Figure 11 shows the linearity characteristics of the first embodiment of the present invention in harmonic distortion form.

As shown in Figure 12, in the first embodiment of the present invention a translinear loop is formed by the third transistor 103, fourth transistor 104, second transistor 102 and first transistor 101. In operation, two sets of current flow into this  
15 first translinear loop which sets up a quiescent current through a branch 170 connected at the collector of the first transistor 101. In addition, as shown in Figure 13, a translinear loop is formed by the seventh transistor 107, the eighth transistor 108, the sixth transistor 106 and the fifth transistor 105. Two sets of current flow in this second translinear loop which sets up a quiescent current through a branch 171  
20 connected at a collector of the fifth transistor 105. These two quiescent currents establish the bias currents for the respective tenth transistor 110 and for the twelfth transistor 112 by means of translinear principles in the loop formed by the ninth transistor 109, eleventh transistor 111, tenth transistor 110 and twelfth transistor 112.

5           When an input voltage is applied to the input  $g_m$  cell 121, an error voltage appears across the output of the input  $g_m$  cell 121 and an error current is produced. Advantageously, the cross-connection of the collector of the second transistor 102 to the emitter of the sixth transistor 106, and the collector of the sixth transistor 106 to the emitter of the second transistor 102 ensures that whatever proportion of the error  
10   current flowing into the emitters of the second transistor 102 and sixth transistor 106 also flows back out through the collectors of the second transistor 102 and the sixth transistor 106 into the bases of the first transistor 101 and the fifth transistor 105. Advantageously, there is no net signal loss in the pre-driver sub-stage translinear loops.

15           The error currents into the bases of the first transistor 101 and the fifth transistor 105, are thus gained up by the pre-driver sub-stage contribution of  $\beta_p$  and  $\beta_n$ . These error currents flow into the translinear loop formed by the ninth transistor 109, eleventh transistor 111, tenth transistor 110 and twelfth transistor 112. These amplified error currents can only flow into the bases of the tenth transistor 110 and  
20   twelfth transistor 112, where they are amplified by the final sub-stage contribution of  $\beta_n$  and  $\beta_p$  respectively. Thus, irrespective of whether the error current flows through the top or the bottom route through the circuit it appears at the output terminal 91 amplified by approximately  $\beta_n$  multiplied by  $\beta_p$ , where it develops a correction

### Output Transistor Biasing

Figure 14 is a circuit diagram of the final sub-stage 123 of the first embodiment of the operational amplifier output stage in a no load configuration. Figure 14 illustrates type I biasing of the output transistors as follows: Current is flowing into the collector of the tenth transistor 110, referred to as  $I_{Q110C}$ , and current is flowing out of the collector of the twelfth transistor 112, referred to as  $I_{Q112C}$ . The emitter area of the ninth transistor 109 is referred to as  $A_{Q109}$  and the emitter area of the eleventh transistor 111 is referred to as  $A_{Q111}$ . The emitter area of the tenth transistor 110 is referred to as  $A_{Q110}$  and the emitter area the twelfth transistor 112 is referred to as  $A_{Q112}$ . Two current sources  $I_{135}$  and  $I_{136}$  are shown thereon:

$$I_{135} = I + \frac{\delta I_{sig}}{2} \text{ and } I_{136} = I - \frac{\delta I_{sig}}{2}$$

**Therefore:**

$$\frac{I_{135}^2}{A_{Q109} * A_{Q111}} = \frac{I_{Q110C} * I_{Q112C}}{A_{Q112} * A_{Q110}}$$

5 for  $\beta_n$  and  $\beta_p \gg 1$  and  $V_{A_n}$  and  $V_{A_p} \gg 1$ ,

$$I_{Q110C} = I_{Q112C} = I_C.$$

$$\text{Therefore, } \frac{I_{135}^2}{A_{Q109} * A_{Q111}} = \frac{I_C^2}{A_{Q112} * A_{Q110}}; \text{ and further}$$

$$I_C = I_{135} \cdot \sqrt{\frac{A_{Q110} * A_{Q112}}{A_{Q109} * A_{Q111}}}$$

10 Figure 15 is a circuit diagram of the final sub-stage 123 of the first embodiment of the present invention with a load 43. Type I biasing of the output transistors is thus described as follows: When a load 43 is connected to the output terminal 91 and the following do not hold:

$$\beta_n \text{ and } \beta_p \gg 1, \text{ or}$$

$$V_{A_n} \text{ and } V_{A_p} \gg 1, \text{ or}$$

15 there is an imbalance between current  $I_{Q110C}$  and  $I_{Q112C}$ .

5           Since current  $I_{Q110C}$  is not equal to  $I_{Q112C}$ , an error current flows in the load 43  
thus developing an offset voltage  $V_{error}$  across the load 43.

When the difference in current in the final sub-stage transistors 110 and 112,  
are taken care of by a localized feedback system, the characteristics of the final sub-  
stage can be seen as follows: The signal current changes the bias currents by  
10   increasing the current through the top circuit and decreasing the current through the  
bottom circuit. In the limiting case for large current through the top circuit and  
miniscule current through the bottom circuit, and  $\alpha$  is equal to one (1), the translinear  
loop cuts off the twelfth transistor 112 and all of the signal current flows into the  
base of the tenth transistor 110 where it appears in the load 43 as follows:

15            $\beta_n * (\delta I_{sig}).$

Conversely, for large signal current through the bottom circuit and miniscule  
current at the top circuit, and where  $\alpha$  is equal to 0, the translinear loop is again cut  
off and all of the signal current flows into the base of the twelfth transistor 112  
where it appears in the load 43 as follows:

20            $\beta_p * (\delta I_{sig}).$

5 For small signal currents, where  $\alpha$  is close to half (.5), the translinear loop is active, that is a quiescent current is flowing through both the tenth transistor 110 and the twelfth transistor 112, the signal current splits with  $\alpha$  and  $(1 - \alpha)$  multiplied by  $\delta I_{sig}$  flowing into the base of the twelfth transistor 112. Thus the current gain from input to output is as follows:

10 
$$\alpha * \beta_n + (1 - \alpha) * \beta_p$$

for all cases of  $\alpha$  such that  $\alpha$  is equal to or greater than zero and equal to or less than 1.

As shown in the graph of Figure 16, the gain will transition from  $\beta_p$  to  $\beta_n$  through the translinear region.

15 Figure 17 is a circuit diagram of the final sub-stage of the second embodiment of an operational amplifier in a no load configuration. Figure 17 illustrates type II biasing of the output transistors as follows:

20 
$$\frac{\beta_n * \beta_p * i_b^2}{A_{Q109} * A_{Q111}} = \frac{I_{Q110C} * I_{Q112C}}{A_{Q112} - A_{Q110}}, \text{ and}$$

25 
$$\frac{\beta_n * \beta_p * i_b^2}{A_{Q109} * A_{Q111}} = \frac{(\beta_n * I - \beta_p * \beta_n * i_b) (\beta I - \beta_n * \beta_p * i_b)}{A_{Q112} - A_{Q110}}$$

5           The current through branch 70 is:  $\beta_p * i_b$ .

The current through branch 75 is:  $I - \beta_p * i_b$ .

The current through branch 72 is:  $\beta_n * i_b$ .

The current through branch 74 is:  $I - \beta_n * i_b$ .

The current through branch 76 is:  $\beta_n * I - \beta_p * \beta_n * i_b$ .

10           The current through branch 77 is:  $\beta_p * I - \beta_n * \beta_p * i_b$ .

As can be seen, an offset current  $(\beta_n - \beta_p) * I$  will develop an offset voltage in a load, and would self correct in the localized feedback circuit.

Referring to Figure 18, which illustrates type II biasing of the output transistors:

15           The current through branch 75 is:  $I + \delta I - \beta_p i_b$ .

The current through branch 74 is:  $I + \delta I - \beta_n i_b$ .

5 The current is through branch 76 is:  $(\beta_n * I) + (\beta_n * \delta I) - (\beta_n * \beta_p * i_b)$ .

The current through branch 77 is:  $(\beta_p * I) - (\beta_p * \delta I) - (\beta_n * \beta_p * \delta I)$ .

Thus, the output current through branch 78 is:  $i_o = I * (\beta_n - \beta_p) + (\beta_n + \beta_p) * \delta I$ .

This result theoretically indicates no crossover distortion in the output, albeit with an offset.

10 Figures 19, 20 and 21 illustrate the-current drive relationships of the type I and type II biasing schemes.

#### Pre-Driver Biasing

Figure 22 is a circuit diagram illustrating one technique of bias current generation for a rail to rail output stage in a conventional operational amplifier. The main disadvantage of this configuration is that current gain from the input to the output is only a single  $\beta$ . Also this type of stage will have a large output impedance making compensation more difficult given variation in a load's impedance. In the first and second embodiments of the present invention, translinear principles are used to establish the bias currents in the pre-driver stage.

15

5 Referring back to Figures 7 and 8, if there is a slight mismatch in the currents through the second transistor 102 and sixth transistor 106 due to an Early voltage mismatch between these two devices, a cascode on the second transistor 102 and the sixth transistor 106 will remedy this effect.

Also referring to Figures 7 and 8, assume that feedback introduces a  
10 correction term into the circuit to establish equality of collector currents in the first transistor 101 and the fifth transistor 105, then:

$$I_{Q101C} = I_{Q105C} = I_{Qpre}$$

Thus, from translinear principles:

$$1. \quad \frac{I_{132}^2}{A_{Q107} * A_{Q108}} = \frac{I_{Q106C}}{A_{Q106}} * \frac{I_{Qpre}}{A_{Qpre}} ;$$

$$15 \quad 2. \quad \frac{I_{132}^2}{A_{Q103} * A_{Q104}} = \frac{I_{Q102C}}{A_{Q102}} * \frac{I_{Qpre}}{A_{Qpre}} ;$$

$$3. \quad I_{Q106C} + I_{Q102C} = I_{131} ;$$

$$4. \quad \frac{I_{132}^2}{A_{Q107} * A_{Q108}} = \frac{A_{Q101}}{I_{Q_{pre}C}} * A_{Q106} = I_{Q106C}; \text{ (derived from equation 1);}$$

$$5. \quad \frac{I_{132}^2}{A_{Q103} * A_{Q104}} = \frac{I_{Q105}}{A_{Q_{pre}C}} * A_{Q102} = I_{Q102C}; \text{ (derived from equation 2);}$$

$$6. \quad \frac{I_{132}^2}{A_{Q107} * A_{Q108}} * \frac{I_{Q105}}{A_{Q_{pre}C}} * A_{Q106} + \frac{I_{132}^2}{A_{Q103} * A_{Q104}} * \frac{A_{Q101}}{I_{Q_{pre}C}} * A_{Q102} = I_{131};$$

(derived from equations 3, 4 and 5)

$$\text{Thus, } I_{Q_{pre}C} = \frac{I_{132}^2}{I_{131}} \left( \frac{A_{Q105} * A_{Q106}}{A_{Q107} * A_{Q108}} + \frac{A_{Q101} * A_{Q102}}{A_{Q103} * A_{Q104}} \right).$$

Referring to the operational amplifier output stage 100 shown in Figure 7, the change in current in the first transistor 101 and the fifth transistor 105 in response to a change in input current is computed as follows: The input current change takes the form of an equal but opposite change in  $I_X$  and  $I_Y$  given that the difference current between  $I_X$  and  $I_Y$  (i.e.  $\delta I$ ) has to be divided between the bases of the first transistor 101 and the fifth transistor 105. Therefore,

$$I_o = I_Y - \alpha * \delta I * \beta_p - I_Y - (1-\alpha) \delta I - \beta_n$$

5 
$$\delta I_o = -\alpha * \delta I * \beta_p - (1-\alpha) * \delta I * \beta_n;$$

$$\delta I_o = -\delta I (\alpha * \beta_p + (1 - \alpha) - \beta_n) .$$

Where  $\alpha$  is greater than zero and less than one, the value of  $\alpha$  indicates the proportion of  $\delta I$  delivered into the bases of each of the pre-driver transistors, first transistor 101 and fifth transistor 105.

10 Where  $\alpha$  is approximately zero,  $I_X$  has significantly increased and  $I_Y$  has significantly decreased by equal and opposite quantities. The base-emitter voltage is large in the second transistor 102 and small in the sixth transistor 106. The second transistor 102 cuts off and all of the difference current between  $I_X$  and  $I_Y$  (i.e.  $\delta I$ ) flows into the base of the fifth transistor 105. This gives a current gain in the circuit  
15 of  $\beta_n$ .

Where  $\alpha$  is approximately equal to one, the opposite of where  $\alpha$  is approximately equal to zero occurs. Where  $I_X$  significantly decreases,  $I_Y$  significantly increases causing all difference current,  $\delta I$ , to flow into base of the first transistor 101, resulting in a current gain of  $\beta_p$ .

5           Where  $\alpha$  is greater than zero but less than one, the pre-driver sub-stage 122 is in translinear mode. The difference current is split in varying proportion into the first transistor 101 and the fifth transistor 105. Thus,  $\delta I_o / \delta I = \alpha * \beta_p + (1 - \alpha) * \beta_n$ .

Referring to Figure 23, the DC response of the pre-driver sub-stage 122 of the present invention is shown.

10           In connection with the coupling of the pre-driver sub-stage 122 to the final sub-stage 123, the biasing scheme of the pre-drivers and the biasing scheme of the final drivers of the present invention have the advantageous property of not absorbing any signal current. All of the signal current is delivered directly into the bases of the transistors, and none is lost in translinear loops.

15           The current gain from the input to the output has approximately the form:

$$\delta I_o \approx \beta_n * \beta_p * \partial I_{in}.$$

5           Feedback Analysis

When feedback is locally applied by means of some localized feedback circuit, the errors are corrected within a very tight loop which will respond much more quickly than relying on the amplifier overall feedback loop.

Four (4) possibilities are presented: (i) current feedback, transitional  $\beta$  output  
10   (ii) current feedback, constant  $\beta$  output (iii) voltage feedback, transitional  $\beta$  output,  
and (iv) voltage feedback, constant  $\beta$  output.

Figure 24 is a circuit diagram of a first embodiment of the present invention with a current feedback circuitry.

Figure 25 is a circuit diagram of the first embodiment of the present invention  
15   with a voltage feedback circuitry.

When the input  $g_m$  cell 121 takes the form of a complementary differential pair, the inherent RHPZ appearing when the pre-driver sub-stage is Miller compensated vanishes as the feed forward term contributing to the RHPZ is pulled back out by the differential pair.

20

5 Figure 28 illustrates the output in a closed loop configuration with [greater than unity gain] driving a heavy load over a wide voltage range. In all cases the worst case non-linearity is approximately plus/minus 1 part in 1000. For the current feedback, constant  $\beta$  output, cross-over distortion is virtually eliminated.

Figure 29 is a circuit diagram of the first embodiment of the present invention  
 10 with a compound darlington output stage using type I biasing. A generalized evaluation of this circuit is as follows:

Referring to current through branches 150, 152, 154 156, 158, 160, 172 and 174 in Figure 29:

Current through branch 150 is  $I_{LTP}$ ; where  $I_{LTP}$  refers to the current through  
 15 current source 131.

Current through branch 152 is:  $-\alpha \cdot \delta I$ .

Current through branch 154 is:  $\frac{I_{LTP}}{2} + \delta I \left( \frac{1}{2} - \alpha \right)$ .

Current through branch 156 is:  $\frac{I_{LTP}}{2} - \frac{\delta I}{2}$ .

Current through branch 158 is:  $\frac{I_{LTP}}{2} + \frac{\delta I}{2}$ .

20 Current through branch 160 is:  $I_{biasp} - \beta_{Q101} \cdot \alpha \cdot \delta I$ .

Current through branch 162 is approximately

equal to:  $I_{biasp} - \frac{I_{LTP}}{2} - \delta I \cdot \beta_{Q101} \cdot \alpha$ .

5 Current through 172 is:  $-\lambda \cdot \delta I (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1-\alpha))$ .

Current through 174 is:

$$-\lambda \cdot \delta I \cdot (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1-\alpha)) + I_{\text{bias out}}.$$

Referring to current through branches 151, 153, 155, 157, 159, 161, 163, 173 and 175:

10 Current through branch 151 is  $I_{LTP}$ ; where  $I_{LTP}$  refers to the current through current source 134 which is the same as the current through current source 131.

Current through branch 153 is:  $(1-\alpha) \delta I$ .

Current through branch 155 is:  $\frac{I_{LTP}}{2} + \delta I \left( \frac{1}{2} - \alpha \right)$ .

Current through branch 157 is:  $\frac{I_{LTP}}{2} + \frac{\delta I}{2}$ .

15 Current through branch 159 is:  $\frac{I_{LTP}}{2} - \frac{\delta I}{2}$ .

Current through branch 161 is:  $I_{\text{bias p}} + \beta_{Q105} \cdot (1-\alpha) \delta I$ .

Current through branch 163 is:  $I_{\text{bias p}} - \frac{I_{LTP}}{2} + \beta_{Q105} \cdot (1-\alpha) \delta I$ .

Current through branch 173 is:  $(1-\lambda) \cdot \delta I (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1-\alpha))$ .

Current through 175 is:  $(1-\lambda) \cdot \delta I (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1-\alpha)) + I_{\text{bias out}}$ .

20

5 Therefore:

$$I_{out} = -\lambda \cdot \delta I \cdot \beta_{Q110} \cdot (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1 - \alpha)) - (1 - \lambda) \cdot \delta I \cdot \beta_{Q112} (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1 - \alpha)) .$$

In a first case where  $I_{out}$  is large and positive, and load conduction is through transistor 110 and transistor 101, where  $\alpha = 1$ ,  $\lambda = 1$ , then:

10  $I_{out} = -\delta I \cdot \beta_{Q110} \cdot \beta_{Q101}$

In a second case where  $I_{out}$  is large and negative, and load conduction is through transistor 112 and transistor 105, where  $\alpha = 0$ ,  $\lambda = 0$ , then:

$$I_{out} = -\delta I \cdot \beta_{Q112} \cdot \beta_{Q105}$$

15

In a third case where  $I_{out}$  is very small through the cross-over point, and load conduction is through transistor 110 and transistor 112, where  $\alpha \approx .5$ ,  $\lambda \approx .5$ , then:

$$I_{out} = -\delta I \left( \frac{\beta_{Q101} + \beta_{Q105}}{2} \right) \left( \frac{\beta_{Q110} + \beta_{Q112}}{2} \right)$$

20 Thus, for  $\beta_{Q112} = \beta_{Q101} = \beta_p$

and  $\beta_{Q110} = \beta_{Q105} = \beta_n$

$$I_{out} = -\delta I \left( \frac{\beta_p + \beta_n}{2} \right)^2$$

Figure 30 is a circuit diagram of the first embodiment of the present invention with a compound darlington output stage using type I biasing and a differential pair input  $g_m$  cell. A specific evaluation of this circuit is as follows:

Referring to the current through branches 140, 142, 152, 160, 172 and 174 in

Figure 30:

The current through branch 140 is:

$$I_{131} + \delta I \left( \frac{1}{2} - \alpha \right)$$

The current through branch 142 is:

$$-\frac{\delta I}{2}$$

The current through branches 152, 160, 172 and 174 are the same as that in the equivalent numbered branches in Figure 29.

Referring to the current through branches 141, 143, 153, 161, 173, and 175 in

Figure 30:

The current through branch 141 is:

$$I_{134} + \delta I \left( \frac{1}{2} - \alpha \right)$$

The current through branch 143 is:

$$\frac{\delta I}{2}$$

5           The current through branches 153, 161, 173 and 175 are the same as that in the equivalent numbered branches in Figure 29.

Therefore:

$$I_{out} = -\lambda \cdot \delta I \cdot \beta_{Q110} \cdot (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1 - \alpha)) - (1 - \lambda) \cdot \delta I \cdot \beta_{Q112} (\beta_{Q101} \cdot \alpha + \beta_{Q105} (1 - \alpha))$$

10           Referring to Figure 30, and as noted in Figure 29, in a first case, where  $I_{out}$  is large and positive, and load conduction is through transistor 110 and transistor 101, where  $\alpha = 1$ ,  $\lambda = 1$ , then:

$$I_{out} = -\delta I \cdot \beta_{Q110} \cdot \beta_{Q101}$$

15           In a second case where  $I_{out}$  is large and negative, and load conduction is through transistor 112 and transistor 105, where  $\alpha = 0$ ,  $\lambda = 0$ , then:

$$I_{out} = -\delta I \cdot \beta_{Q112} \cdot \beta_{Q105}$$

20           In a third case, where case  $I_{out}$  is very small through the cross-over point, and load conduction is through transistor 110 and transistor 112, where  $\alpha \approx .5$ ,  $\lambda \approx .5$ , then:

$$I_{out} = -\delta I \left( \frac{\beta_{Q101} + \beta_{Q105}}{2} \right) \left( \frac{\beta_{Q110} + \beta_{Q112}}{2} \right)$$

Thus, for  $\beta_{Q112} = \beta_{Q101} = \beta_p$

5

and  $\beta_{Q110} = \beta_{Q105} = \beta_n$

$$I_{out} = -\delta I \left( \frac{\beta_p + \beta_n}{2} \right)^2$$

where  $0 < \alpha < 1$ ;

10 and  $0 < \lambda < 1$ .

$I_{biasp}$  and  $I_{biasout}$  are established using translinear principles.

### Compensation

Figures 31, 32, 33 and 34 show the various types of compensation techniques  
 15 that can be used with the present invention. Figure 31 is a half circuit showing the  
 current feedback case with small signal AC. The circuit is a 2 voltage gain stage  
 amplifier with voltage gain being developed at nodes 63 and 64. The circuit lends  
 itself to classic Miller compensation as shown in Figure 31.

Referring to Figure 32, the resistor 81 eliminates the right half plane through  
 20 the compensation capacitor 85. At the quiescent condition, the value is the reciprocal  
 of the transconductance of the first transistor 101.

Figure 33 illustrates the voltage feedback case. Referring to the circuit in  
 Figure 33, there are two (2) loops to be compensated, inner loop 2 and outer loop 1.  
 As can be seen in Figure 32, similar to the current feedback implementation, the

5 system is a 2 voltage gain stage amplifier with voltage gain at nodes 63 and 64. This circuit can also be Miller compensated. There is no concern with RHPZ because the differential transistor 113 draws the feed forward signal out.

#### Implementation

It is noted that the voltage feedback implementation can only be used for gain  
10 greater than 1. Further, the current feedback implementation can be used for arbitrary gain. All four implementations can be used as a stand alone amplifier configuration.

Figure 35 illustrates how gain from the present invention can be preserved where additional lower frequency precision is required.

15 The advantages of the present invention over conventional operational amplifier output stages is significantly higher linearity for the same supply current or linearity equal to the conventional operational amplifiers.

The current gain obtained in the error correction loop of each of the first and second conventional operational amplifiers is only a single current gain whereas the  
20 current gain of the present invention is up to  $\beta^2$ . Further, the DC non-linearity of conventional amplifiers is approximately 2 parts per 1000, a factor of 25 worse than the present invention. Reduced current draw is one of the advantages afforded by the design of each of the present invention.

The numerous innovative teachings of the present application are described  
25 with particular reference to the disclosed embodiments. However, it should be

5 understood that these embodiments provide only two examples of the many  
advantageous uses and innovative teachings herein. Various alterations,  
modifications and substitutions can be made to the disclosed invention without  
departing in any way from the spirit and scope of the invention, as defined in the  
claims that follow. For example, although the embodiments have been presented  
10 herein with reference to particular transistor types, voltage and current polarities and  
methods of coupling, the present inventive structures and characteristics are not  
necessarily limited to particular transistor types, polarities or methods of coupling, as  
used herein. It should be understood the embodiment used hereinabove can easily be  
implemented using many diverse transistor types, polarities and methods of coupling  
15 so long as the combinations achieve an ultra linear, high speed operational amplifier  
output stage with reduced current draw and extended bandwidth.